II. Amendment to the Claims

Claims 1-22 are pending. No amendments to the claims are made herein, although a reformatted listing of claims is provided below as requested by the Examiner. This listing and version of the claims replaces all prior listings and versions of the claims.

1. (original) A circuit operable to measure leakage current in a Dynamic Random Access Memory (DRAM) comprising:

a plurality of DRAM bit cell access transistors coupled to a common bit line, a common word line, and a common storage node, wherein said access transistors may be biased to simulate a corresponding plurality of inactive bit cells of a DRAM; and

a current mirror in communication with said common storage node operable to mirror a total leakage current from said plurality of bit cell access transistors when said access transistors are biased to simulate said inactive bit cells.

2. (original) The circuit as recited in claim 1, wherein said access transistors are selected from the group consisting of NMOS and PMOS transistors.

3. (original) The circuit as recited in claim 1, wherein said current mirror comprises:

at least two transistors with respective gate nodes electrically connected to said common storage node.

4. (original) The circuit as recited in claim 3, wherein said current mirror transistors are selected from the group consisting of NMOS and PMOS transistors.

5. (original) The circuit as recited in claim 3, wherein said current mirror transistors are selected to measure a multiple of said total leakage current, said multiple being greater than one.

6. (original) The circuit as recited in claim 3, wherein said current mirror comprises at least two NMOS transistors coupled between said common storage node and a ground node, whereby a voltage at said common storage node simulates a voltage reflective of a '0' state DRAM bit cell when said access transistors are biased to simulate said inactive bit cells.

7. (original) The circuit as recited in claim 3, wherein said current mirror comprises at least two PMOS transistors coupled between said common storage node and a supply voltage node, whereby a voltage at said common storage node simulates a voltage reflective of a '1' state DRAM bit cell when said access transistors are biased to simulate said inactive bit cells.

8. (original) The circuit as recited in claim 1, further comprising a plurality of storage capacitors coupled to said storage node, each of said storage capacitors associated with a respective one of said access transistors, wherein said current mirror is operable to mirror a total leakage current from said plurality of bit cell access transistors and said capacitors.

9. (original) A DRAM current meter comprising:

a first current monitor operable to measure a leakage current associated with a cell in a first state;

a second current monitor operable to measure a leakage current associated with a cell in a second state; and

a current mirror in communication with said first and second current monitors wherein said current mirror is operable to mirror a total leakage current measured by said first and second current monitors.

10. (original) The meter as recited in claim 9, wherein said second current monitor provides a current to said current mirror.

11. (original) The meter as recited in claim 10, wherein said current mirror is a current sink for said first current monitor.

12. (original) The meter as recited in claim 9, wherein each of said first and second current monitors comprises:

a plurality of DRAM bit cell access transistors coupled to a common bit line, a common word line, and a common storage node, wherein said access transistors may be biased to simulate a corresponding plurality of inactive bit cells of a DRAM; and

a current mirror in communication with said common storage node operable to mirror a total leakage current from said plurality of bit cell access transistors when said access transistors are biased to simulate said inactive bit cells.

13. (original) The meter as recited in claim 12, wherein said each current mirror of said first and second current monitors comprises:

at least two transistors with respective gate nodes electrically connected to said common storage node.

14. (original) The meter as recited in claim 13, wherein said transistors of said current mirrors of said first and second current monitors are selected to measure a multiple of said total leakage current, said multiple being greater than one.

15. (original) The meter as recited in claim 13,

wherein said current mirror of said first current monitor comprises at least two NMOS transistors coupled between said common storage node and a ground node, whereby a voltage at said common storage node simulates a voltage reflective of a '0' state DRAM bit cell when said access transistors are biased to simulate said inactive bit cells, and

wherein said current mirror of said second current monitor comprises at least two PMOS transistors coupled between said common storage node and a supply voltage node,

whereby a voltage at said common storage node simulates a voltage reflective of a '1' state DRAM bit cell when said access transistors are biased to simulate said inactive bit cells.

16. (original) The meter as recited in claim 12, wherein said current mirrors of said first and second current monitors each further comprise:

a plurality of storage capacitors coupled to said storage node, each of said storage capacitors associated with a respective one of said access transistors, wherein said current mirror is operable to mirror a total leakage current from said plurality of bit cell access transistors and said capacitors.

17. (original) A Dynamic Random Access Memory (DRAM) comprising a circuit operable to measure simulated leakage current in said DRAM comprising:

a plurality of DRAM bit cells comprising:

a plurality of DRAM bit cell access transistors coupled to a common bit line, a common word line, and a common storage node, wherein said access transistors may be biased to simulate a corresponding plurality of inactive bit cells of a DRAM; and

a plurality of storage capacitors coupled to said storage node, each of said storage capacitors associated with a respective one of said access transistors; and

a current mirror in communication with said common storage node operable to provide a multiple of a total leakage current from said plurality of bit cell access transistors and said capacitors when said access transistors are biased to simulate said inactive bit cells.

18. (original) The DRAM of claim 17, wherein said current mirror comprises:

at least two transistors with respective gate nodes electrically connected to said common storage node.

19. (original) The DRAM of claim 18, wherein said current mirror comprises at least two NMOS transistors coupled between said common storage node and a ground node, whereby a voltage at said common storage node simulates a voltage reflective of a '0' state DRAM bit cell when said access transistors are biased to simulate said inactive bit cells.

20. (original) The DRAM of claim 18, wherein said current mirror comprises at least two PMOS transistors coupled between said common storage node and a supply voltage node, whereby a voltage at said common storage node simulates a voltage reflective of a '1' state DRAM bit cell when said access transistors are biased to simulate said inactive bit cells.

21. (original) The DRAM of claim 17, wherein said DRAM comprises a DRAM array and said circuit is fabricated proximate to said DRAM array, whereby said circuit is exposed to environmental conditions substantially similar to said DRAM memory array.

22. (original) The DRAM of claim 17, wherein said multiple is greater than one.